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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,862	06/16/2006	John Christopher Rudin	20030814-3	4120

22879 7590 03/17/2009

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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
03/17/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/564,862	RUDIN, JOHN CHRISTOPHER	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,7-10,14,18,19,22-25,29,31,35,36,42,44 and 49* is/are pending in the application.

4a) Of the above claim(s) *25,29,31,35,36,42,44 and 49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,7-10,14,18,19 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/12/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1, 5, 7 - 10, 14, 18, 19, and 22 - 24 in the reply filed on December 4, 2008 is acknowledged. Claims 25, 29, 31, 35, 36, 42, 44, and 49 are withdrawn from consideration.

Specification

2. The abstract of the disclosure is objected to because it is filed as part of the PCT publication, containing information not related to the abstract. Furthermore, the abstract is not written in narrative form, but rather reads as legal phraseology. Correction is required. See MPEP § 608.01(b).

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "*dielectric material*" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 14 depends from Claim 10, which recites a dielectric layer "*between the fourth layer and third layer*." As seen in figure 3B dielectric layer 112 is between the fourth layer 106 comprising the gate electrode and the third layer 114 comprising the substrate. However, the dielectric layer 112 of claim 10, as seen in figure 3B, does not separate the source and drain electrodes from the gate electrode. Instead, a second dielectric layer 122 separates the source and drain electrodes from the fourth layer 106 comprising the gate electrode. Therefore, the "*dielectric material*" of claim 14 is interpreted as "*a second dielectric layer*".

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 5, and 7 – 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Aratani et al. (US 5,705,826).

a. Regarding claim 1, **Aratani discloses a semiconductor device** (e.g. figure 1) **comprising:**

a first electrode component (source electrode 6);

a second electrode component (drain electrode 5);

a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component (e.g. top layer comprising first and second electrode components 5 and 6);

a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components (semiconductor layer 4, disclosed in col. 11, line 11); **and**

a third layer comprising a substrate (substrate 1),

wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer (e.g. as seen in figure 1, second layer 4 is between first layer comprising components 5 and 6, and third layer 1) **and**

wherein the first and second electrode components comprise electro-deposited metal (col. 11, lines 14 – 15 disclose the first and second electrode components (source and drain electrodes) are made of gold.

Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components are metal (gold) and therefore anticipate the structural limitation, regardless of how that structure is formed).

b. Regarding claim 5, **Aratani discloses a semiconductor device as claimed in claim 1, wherein the deposited semiconductor material comprises organic semiconductor material** (e.g. as disclosed in col. 6, lines 35 - 36, col. 8, lines 36 - 37, col. 10, lines 49 - 51 (Synthesis Example 1), and col. 11, lines 11 - 13).

c. Regarding claim 7, **Aratani discloses a semiconductor device as claimed in claim 1, wherein the semiconductor material is embedded in the device and overlain by the first layer** (e.g. as seen in figure 1, the semiconductor material of layer 4 is embedded in the device and overlain by the first layer comprising electrodes 5 and 6).

d. Regarding claim 8, **Aratani discloses a semiconductor device as claimed in claim 1, wherein the substrate is flexible** (e.g. col. 6, lines 10 - 19).

e. Regarding claim 9, **Aratani a semiconductor device as claimed in claim 1, wherein the device is a thin film transistor** (e.g. as disclosed in the

title) **having a channel in the semiconductor material** (e.g. channel region in semiconductor layer 4 between drain and source electrodes 5 and 6), **a source electrode as the first electrode** (source electrode 6, disclosed in col. 11, line 14), **a drain electrode as the second electrode** (drain electrode 5, disclosed in col. 11, line 14), **and a gate electrode** (gate electrode 2, disclosed in col. 11, line 8), **wherein the source, drain and gate electrodes are formed from electro-deposited metal** (col. 11, lines 5 - 8 disclose the gate to be formed of chromium, and col. 11, lines 14 – 15 disclose the source and drain electrodes are made of gold. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components are metal and therefore anticipate the structural limitation, regardless of how that structure is formed).

9. Claims 1, 9, 10, 14, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (US 6,013,930).

a. Regarding claim 1, **Yamazaki discloses a semiconductor device** (e.g. figures 1A – 2B and 5A – 5C) **comprising:**

a first electrode component (source electrode 501);

a second electrode component (drain electrode 502);

a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component (e.g. top layer comprising first and second electrode components 501 and 502);

a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components (second layer comprising semiconductor material 503 and the remaining semiconductor layer 111, disclosed in col. 14, lines 30 – 33 and col. 12, lines 25 – 27); **and**

a third layer comprising a substrate (substrate 101),

wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer (e.g. as seen in figure 1, second layer comprising layers 111 and 503 is between first layer comprising components 501 and 503, and third layer 101) **and**

wherein the first and second electrode components comprise electro-deposited metal (e.g. col. 11, lines 58 - 62 disclose the first and second electrode components (source and drain electrodes) are made of titanium and aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components are metal (titanium and aluminum) and therefore anticipate the structural limitation, regardless of how that structure is formed).

b. Regarding claim 9, **Yamazaki discloses a semiconductor device as claimed in claim 1, wherein the device is a thin film transistor** (e.g. as disclosed in col. 14, line 18) **having a channel in the semiconductor material**

(e.g. channel region 503, disclosed in col. 14, line 33), **a source electrode as the first electrode** (source electrode 501, disclosed in col. 14, lines 24 - 25), **a drain electrode as the second electrode** (drain electrode 502, disclosed in col. 14, line 25), **and a gate electrode** (gate electrode 103, disclosed in col. 8, line 13), **wherein the source, drain and gate electrodes are formed from electro-deposited metal** (col. 8, lines 13 - 16 disclose the gate to be formed of various metals, and col. 11, lines 58 – 62 disclose the source and drain electrodes are made of titanium and aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components are metal and therefore anticipate the structural limitation, regardless of how that structure is formed).

c. Regarding claim 10, **Yamazaki discloses a semiconductor device as claimed in claim 9, wherein the first layer comprises the source electrode and the drain electrode** (e.g. as seen in the figures, source electrode 501 and drain electrode 502 reside the in first layer which comprises the source and drain electrodes) **and the gate electrode lies in a fourth layer between the second layer and the third layer** (e.g. gate electrode 103 lies in fourth layer 105, as seen in figure 1A, which is between the second layer comprising 503 and 111, and the third layer 101), **the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer** (fifth layer 102, which is between the fourth layer 105 and

third layer 101, as seen in figure 1A. Col. 8, lines 3 – 4 disclose the layer to be an insulating layer).

d. Regarding claim 14, **Yamazaki discloses a semiconductor device as claimed in claim 10, wherein the source and drain electrodes each partially overlap the gate electrode** (e.g. as seen in figure 5B, the source and drain electrodes 501 and 502 overlap the gate electrode 103) **but are separated therefrom by the semiconductor material and a second dielectric layer** (e.g. as seen in figure 5B, the source and drain electrodes 501 and 502 are separated from the gate 103 by the semiconductor material 503 and a second dielectric layer 106, as disclosed in figure 106 and col. 8, line 30).

e. Regarding claim 24, **Yamazaki discloses a substrate for a display device comprising a plurality of semiconductor devices as claimed in claim 1** (e.g. figure 12A - 15D, and disclosed in Embodiment 10, col. 20, line 19).

10. Claims 1, 9, 18, 19, 22, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Noguchi et al. (US 5,183,780).

a. Regarding claim 1, **Noguchi discloses a semiconductor device** (e.g. figure 4G) **comprising:**

a first electrode component (source electrode comprising parts 26 (left side) and 28);

a second electrode component (drain electrode comprising parts 26 (right side) and 29);

a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component (e.g. top layer comprising first and second electrode components 28, 29, and 30, formed in figure 4F from layer 27);

a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components (semiconductor material 21 and contacts 26, disclosed in col. 7, line 39); **and**

a third layer comprising a substrate (substrate 20),

wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer (e.g. as seen in figure 4G, second layer 21 is between first layer comprising components 28 and 29, and third layer 20) **and**

wherein the first and second electrode components comprise electro-deposited metal (col. 8, lines 18 – 23 disclose the first and second electrode components (source and drain electrodes) comprise aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components comprise metal (aluminum) and therefore anticipate the structural limitation, regardless of how that structure is formed).

b. Regarding claim 9, **Noguchi discloses a semiconductor device as claimed in claim 1, wherein the device is a thin film transistor** (e.g. as disclosed in col. 7, line 36) **having a channel in the semiconductor material** (e.g. channel region in semiconductor layer 21 between drain and source electrodes 26), **a source electrode as the first electrode** (source electrode 28, disclosed in col. 8, line 21), **a drain electrode as the second electrode** (drain electrode 29, disclosed in col. 8, line 22), **and a gate electrode** (gate electrode 30, disclosed in col. 8, line 22), **wherein the source, drain and gate electrodes are formed from electro-deposited metal** (col. 8, lines 18 – 23 disclose the source, drain, and gain electrodes are formed from aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components comprise metal (aluminum) and therefore anticipate the structural limitation, regardless of how that structure is formed).

c. Regarding claim 18, **Noguchi discloses a semiconductor device as claimed in claim 9, wherein the first layer comprises a first portion of the source electrode, a first portion of the drain electrode and the gate electrode** (e.g. as seen in figure 4, and cited above with respect to claim 1, the first layer comprises the portions of the source electrode 28, portions of the drain electrode 29, and the gate electrode 30).

d. Regarding claim 19, **Noguchi discloses a semiconductor device as claimed in claim 18, wherein the second layer comprises a second portion of the source electrode contacting the semiconductor material and a second portion of the drain electrode contacting the semiconductor material** (e.g. as seen in figure 4, and cited above with respect to claim 1, the second layer comprises portions of the source and drain electrode (contact portions 26), which contact the semiconductor material 21).

e. Regarding claim 22, **Noguchi discloses a semiconductor device as claimed in claim 18, further comprising dielectric material in the second layer between the semiconductor material and the gate electrode in the first layer** (dielectric material 22, disclosed in col. 7, line 40).

f. Regarding claim 23, **Noguchi discloses a semiconductor device as claimed in claim 18, wherein the first layer has a substantially planar surface forming a surface of the semiconductor device incorporating portions of the source, drain and gate electrodes** (e.g. as seen in figure 4G, and disclosed in col. 8, lines 20 - 23, the first layer comprises portions 28 of the source, 29 of the drain, and 30 of gate, which are substantially coplanar with each other).

Double Patenting

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

12. Claims 1, 5, 7, 9, 18, 19, 22, and 23 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2, 5, 6, 8, 9, and 25 of copending Application No. 10/563,679. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the copending application disclose all of the structural limitation of the cited claims of the current application, including the first, second, and third layers, the source, drain, and gate metal electrodes, the organic substrate, the semiconductor material, the insulating layer between the semiconductor material and gate electrode, and the relative relationships and positions between all of the claimed structures.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 2892
March 4, 2009

/Lex Malsawma/
Primary Examiner, Art Unit 2892